STLVDS9637

HIGH SPEED DIFFERENTIAL LINE RECEIVERS

- MEETS OR EXCEEDS THE REQUIREMENTS OF ANSI TIA/EIA-644 STANDARD
- OPERATES WITH A SINGLE 3.3V SUPPLY
- DESIGNED FOR SIGNALING RATE UP TO 400Mbps
- DIFFERENTIAL INPUT THRESHOLDS ±100mV MAX
- TYPICAL PROPAGATION DELAY TIME OF 2.5ns
- POWER DISSIPATION 60mW TYPICAL PER RECEIVER AT 200MHz
- LOW VOLATGE TTL (LVTTL) LOGIC OUTPUT LEVELS
- OPEN CIRCUIT FAIL SAFE
- ESD PROTECTION:
  7KV RECEIVER PINS
  3KV ALL PINS VS GND

SOP

DESCRIPTION

The STLVDS9637, is a differential line receiver that implements the electrical characteristics of low voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds and allow operations with a 3.3V supply rail. This differential receiver provides a valid logical output state with a 3.3V supply rail. It also provides a valid logical output state with a ±100mV differential input voltage within the input common mode voltage range. The input common mode voltage allows 1V of ground potential difference between two LVDS nodes.

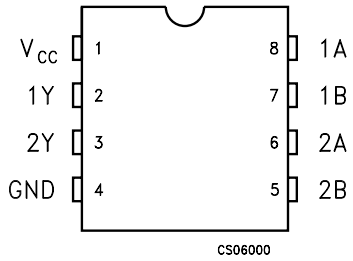
The intended application of this device and signalling technique is both point-to-point and multidrop data transmission over controlled impedance media approximately 100Ω. The transmission media may be printed circuit board traces, backplanes or cables. The ultimate rate and distance of data transfer depend upon the attenuation characteristics of the media and noise coupling to the environment.

The STLVDS9637 version is characterized for operation from -40°C to 85°C.

ORDERING CODES

Type	Temperature Range	Package	Comments
STLVDS9637BD	-40 to 85 °C	SO-8 (Tube)	100parts per tube / 40tube per box
STLVDS9637BDR	-40 to 85 °C	SO-8 (Tape & Reel)	2500 parts per reel

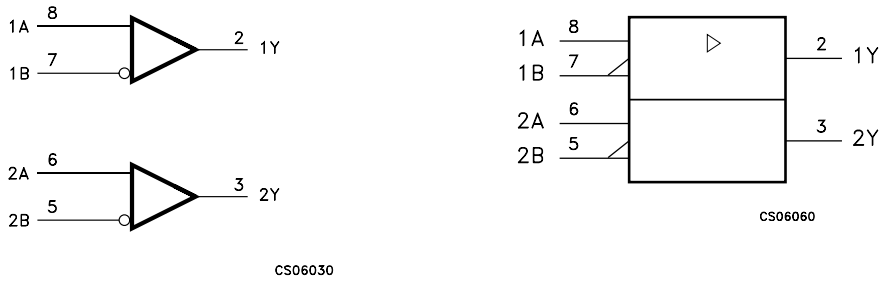
PIN CONFIGURATION



PIN DESCRIPTION

PIN N°	SYMBOL	NAME AND FUNCTION
2, 3	1Y to 2Y	Receiver Outputs
5, 7	1B to 2B	Negated Receiver Inputs
6, 8	1A to 2A	Receiver Inputs
4	GND	Ground
1	V_{CC}	Supply Voltage

LOGIC DIAGRAM AND LOGIC SYMBOL



TRUTH TABLE

DIFFERENTIAL INPUTS	OUTPUT
A, B	**Y**
$V_{ID} \geq 100mV$	H
$-100mV < V_{ID} < 100mV$	?
$V_{ID} \leq -100mV$	L
OPEN	H

L = Low level, H = High Level, X = Don't care, Z = High Impedance, ? = Indeterminate

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (Note 1)		-0.5 to 4.6	V
V_I	Input Voltage		-0.5 to (V_{CC} + 0.5)	V
V_I	Input Voltage (A or B inputs)		-0.5 to 4.6	V
ESD	Human Body Model	Pins Receivers	7	KV
		All Pins vs GND	3	
T_{stg}	Storage Temperature Range		-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.
Note 1: All voltages except differential I/O bus voltage, are with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	HIGH Level Input Voltage (ENABLE)	2.0			V
V_{IL}	LOW Level Input Voltage (ENABLE)			0.8	V
$\|V_{ID}\|$	Magnitude of Differential Input Voltage	0.1		0.6	V
V_{IC}	Common Mode Input Voltage	$0.5\|V_{ID}\|$		$2.4-0.5\|V_{ID}\|$	V
				V_{CC} - 0.8	
T_A	Operating Temperature Range	-40		85	°C

ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{CC} = 3.3V)

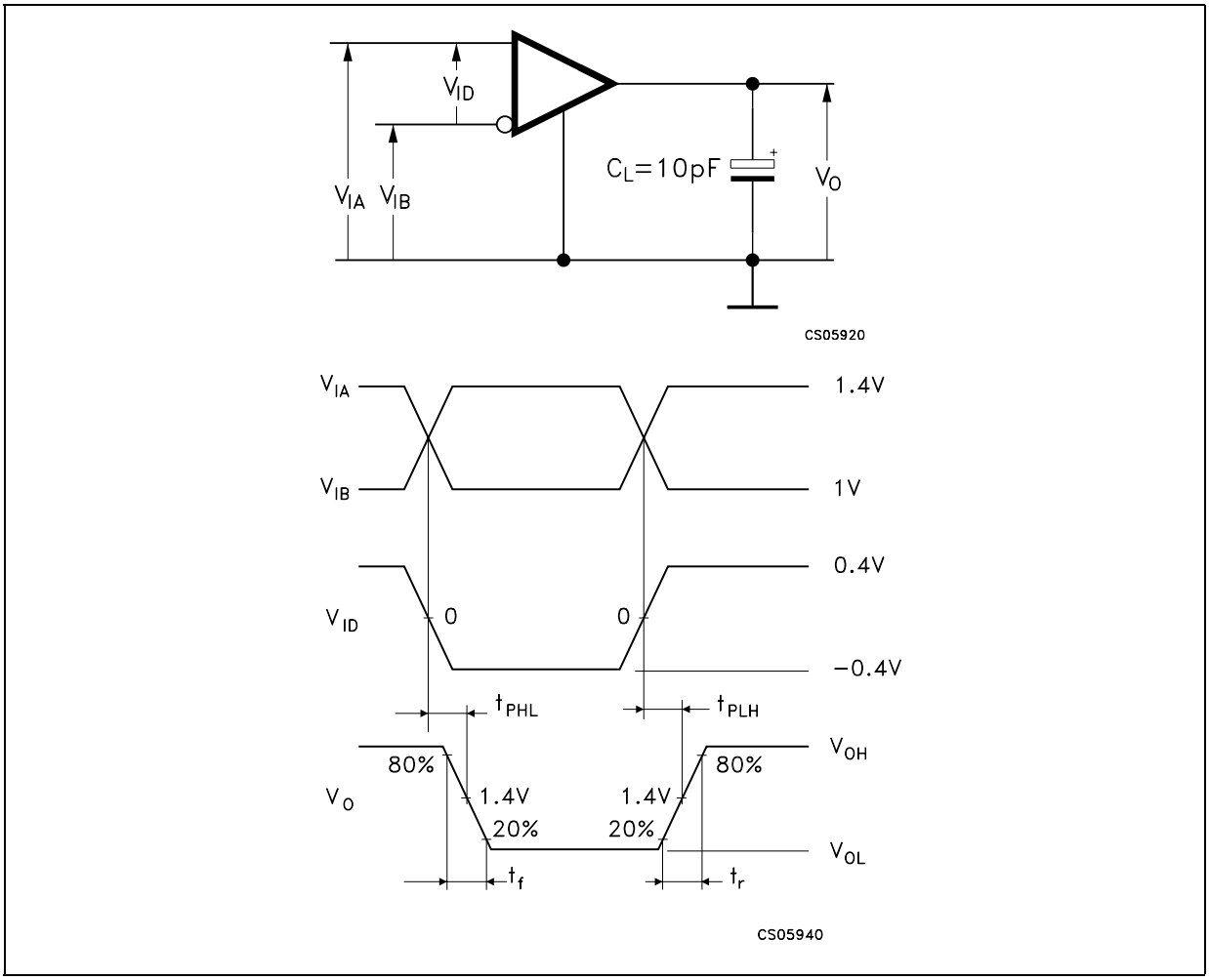
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ITH+}	Positive Going Differential Input Voltage Threshold				100	mV
V_{ITH-}	Negative Going Differential Input Voltage Threshold		-100			mV
V_{OH}	High Level Output Voltage	I_{OH} = -8mA	2.4			V
		I_{OH} = -4mA	2.8			
V_{OL}	Low Level Output Voltage	I_{OH} = 8mA			0.4	V
I_{CC}	Supply Current for STLVDS32, STLVDS3486	Enabled, No Load		10	18	mA
		Disabled		0.25	0.5	mA
I_{CC}	Supply Current for STLVDS9637	No Load		4	10	mA
I_I	Input Current (A or B inputs)	V_I = 0V	-2	-10	-20	µA
		V_I = 2.4V	-1.2	-3		
$I_{I(OFF)}$	Power off Input Current (A or B inputs)	V_{CC} = 0 V_I = 3.6V		10	20	µA
I_{IH}	High Level Input Current (EN, G, $\overline{G}$ or Inputs)	V_{IH} = 2V			10	µA
I_{IL}	Low Level Input Current (EN, G, $\overline{G}$ or Inputs)	V_{IL} = 0.8V			10	µA
I_{OZ}	High Impedance Output Current	V_O = 0 or V_{CC}			± 10	µA

SWITCHING CHARACTERISTICS (Unless otherwise noted. Typical values are referred to T_A = 25°C and V_{CC} = 3.3V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay Time, Low to High Output	C_L = 10pF Fig. 1	1.5	2.5	3.3	ns
t_{PHL}	Propagation Delay Time, High to Low Output		1.5	2.5	3.3	ns
t_r	Differential Output Signal Rise Time			0.4		ns
t_f	Differential Output Signal Fall Time			0.4		ns
$t_{sk(O)}$	Channel to Channel Output Skew (note1)			0.1	0.3	ns
$t_{sk(P)}$	Pulse Skew ($\|t_{PHL} - t_{PLH}\|$) (note2)			0.2	0.4	ns
$t_{sk(PP)}$	Part to Part Skew (note3)				1	ns
t_{PZH}	Propagation Delay Time, High Impedance to High Level Output	Fig. 2		3	12	ns
t_{PZL}	Propagation Delay Time, High Impedance to Low Level Output			5	12	ns
t_{PHZ}	Propagation Delay Time, High Level to High Impedance Output			5	12	ns
t_{PLZ}	Propagation Delay Time, Low Level to High Impedance Output			5	12	ns

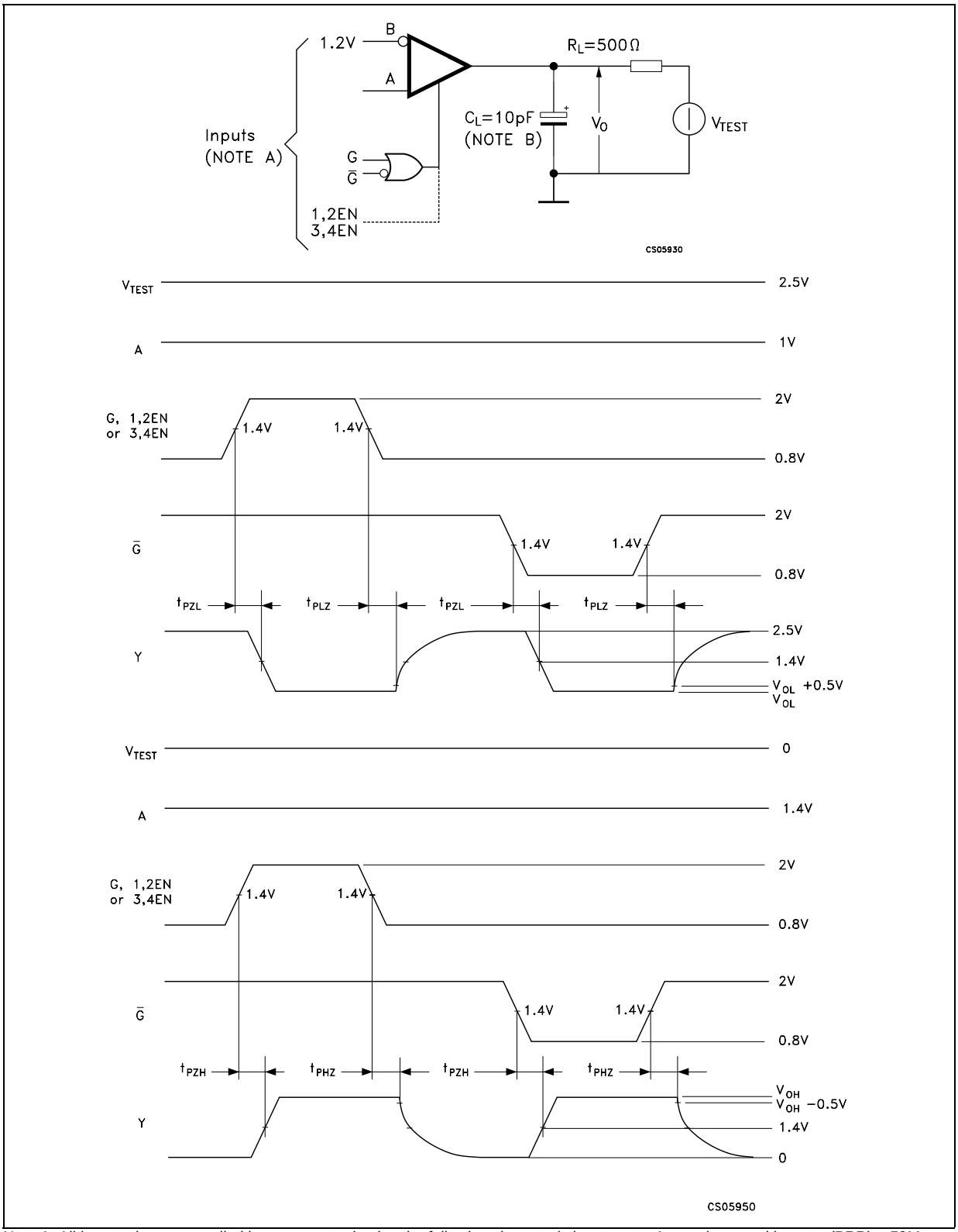
Note 1: $t_{sk(O)}$ is the maximum delay time difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
Note 2: $t_{sk(P)}$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
Note 3: $t_{sk(PP)}$ is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.

Figure 1 : Timing Test Circuit, Timing And Waveforms



Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 10 ± 0.2ns.
Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

Figure 2 : Enable And Disable Time Test Circuit And Waveform



Note A: All input pulse are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, pulse repetition rate (PRR) = 50Mpps, pulse width = 500 ± 10ns.
Note B: C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 3 : Output Current vs Output Voltage

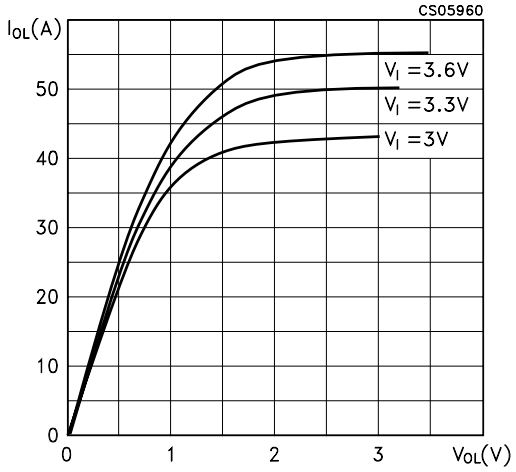
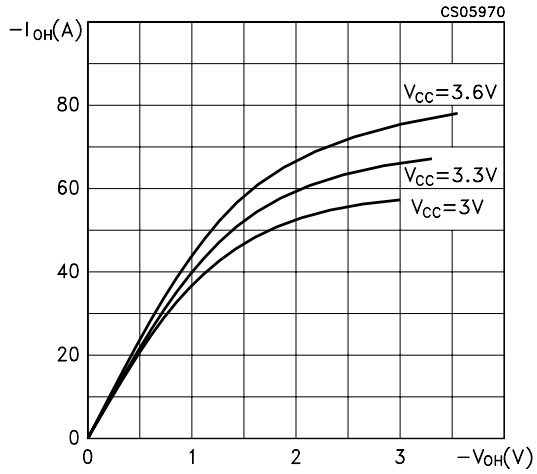
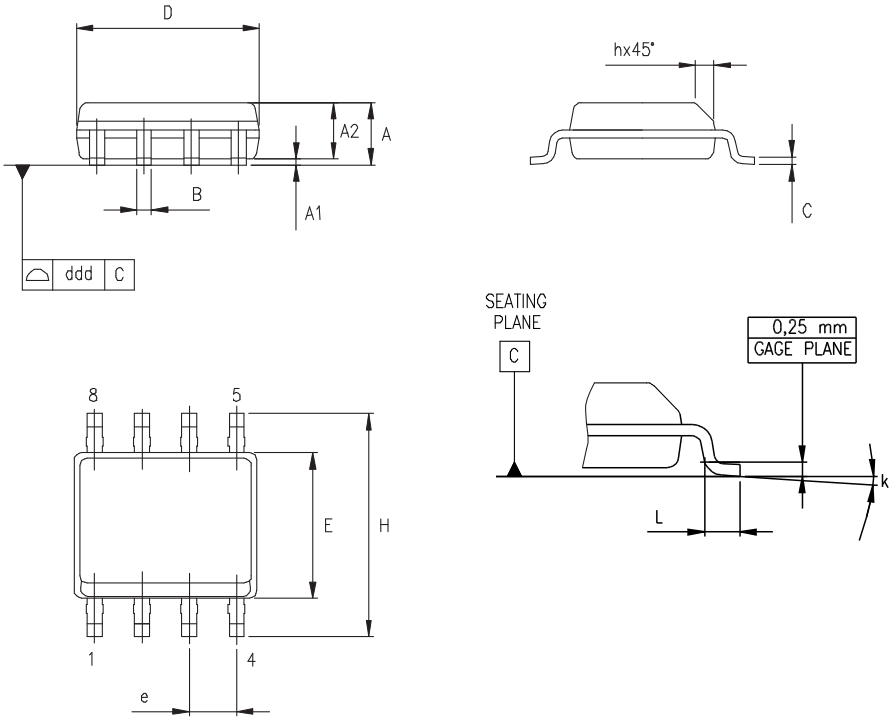


Figure 4 : Output Current vs Output Voltage



SO-8 MECHANICAL DATA

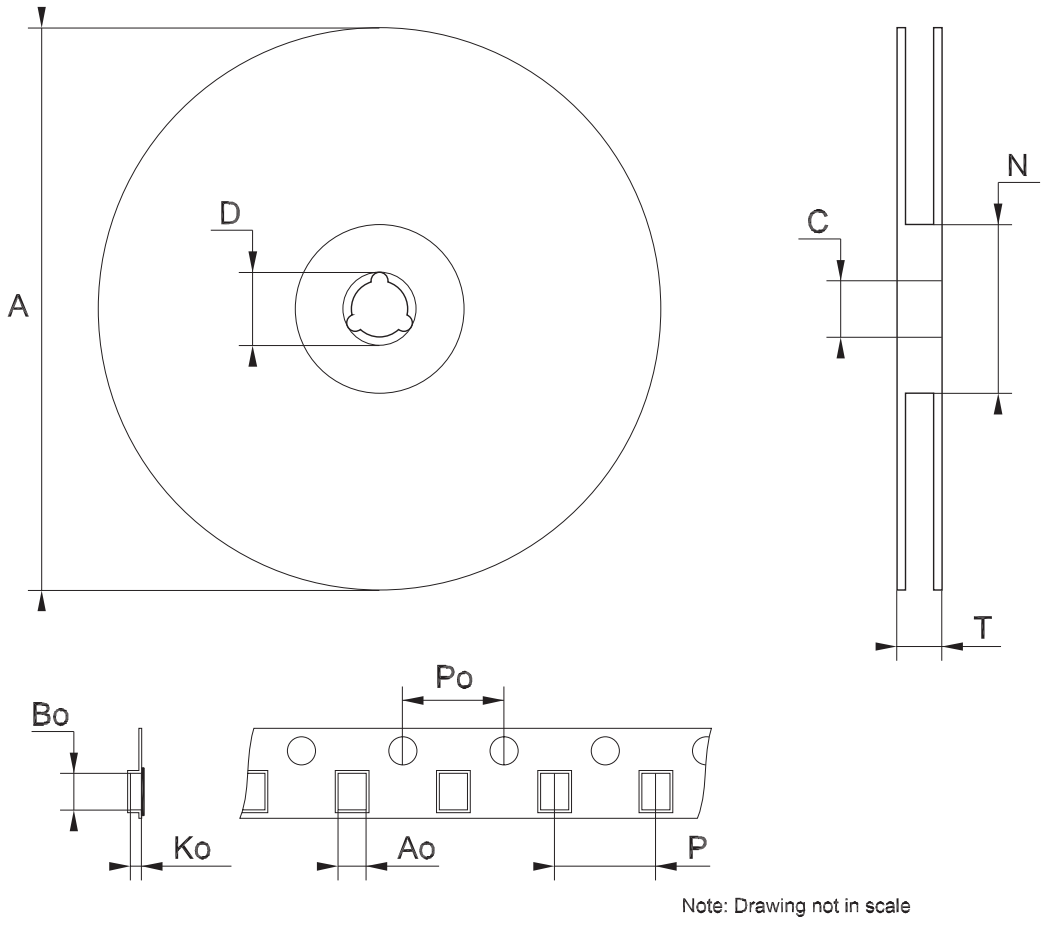
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



0016023/C

Tape & Reel SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	8.1		8.5	0.319		0.335
Bo	5.5		5.9	0.216		0.232
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale